In the specification

Paragraph 38 is as follows based on the amendment herein.

Turning to FIGS. 5 - 7, thick S/D structures 220 may be formed recessed below opposite sides of the gate stack. Referring particularly to FIG. 5 and according to step 120, an un-masked etch selective to nitride is performed that etches through semiconductor layer 208, STI 210, and oxide layer 206. Accordingly, the etch may stop on nitride layer 204. Nitride cap 216 protects the gate stack during this etch. In this manner, recesses for the S/D structures 220 are formed in the semiconductor layer 208, thereby forming a transistor body from a portion of the semiconductor layer 208 situated between the recesses so that a top body surface and a bottom body surface define a body thickness. Referring particularly to FIG. 6 and according to step 122, S/D structure 220 material, such as polysilicon, is then deposited and planarized with the top of the gate stack.

Paragraph 41 is as follows based on the amendment herein.

Thus, in FIG. 7, an embodiment of the present invention is depicted having a minimum of complexity. This depicted embodiment of the present invention is at a stage of a process flow technique modified by a fabrication method of the present invention for forming a transistor structure with thick recessed S/D structures 220. Particularly in this embodiment, semiconductor wafer 200 is depicted with an overlying oxide layer 202. On top of oxide layer 202 is nitride layer 204. Overlying a relevant portion of nitride layer 204 is oxide layer 206. On top of oxide layer 206 is semiconductor layer 208 (i.e. the transistor body), which underlies a gate stack comprising gate oxide layer 212, gate conductor layer 214 overlying gate oxide layer 212, and a

nitride cap 216 overlying gate conductor layer 214. Side wall spacers 218 are adjacent the gate stack. Recesses are formed through semiconductor layer 208 and oxide layer 206 stopping on nitride layer 204 so that semiconductor layer 208 and the gate stack are situated between the recesses. STI isolations comprising STI 222 and S/D structures 220 are formed into the recesses and therefore the S/D structures 220 are at least as thick as a combination of the semiconductor layer 208 and oxide layer 206. S/D structures 220 are formed into the recesses to facilitate lowering the S/D regions in order to decrease S/D resistance. Accordingly, top portions of S/D structures 220 are recessed below gate oxide layer 212 within the thickness of semiconductor layer 208 situated between the recesses and abutting semiconductor layer 208.